# CLAIMS

1. A method of evaluating an integrated circuit having a plurality of data terminals from which data signals are transmitted, the method comprising:

capacitively coupling a test plate to a plurality of signal terminals from which data signals are transmitted;

transmitting a data signal from one of the plurality of signal terminals; and

evaluating the data signal detected by the test plate against a test criteria.

2. The method of claim 1, further comprising placing the remaining data terminals of the plurality in a high-impedance state.

3. The method of claim 1 wherein the transmitting signal terminal is a first signal terminal, and the method further comprises:

ceasing transmission of the data signal from the first signal terminal;

transmitting a data signal from another one of the plurality of signal terminals; and

evaluating the data signal detected by the test plate against the test criteria.

4. The method of claim 1 wherein the integrated circuit is formed on a semiconductor die and capacitively coupling a test plate comprises:

forming the test plate from a conductive plate layer formed on the semiconductor die; and

forming data terminals from conductive signal pads and in proximity to the conductive plate layer, the conductive plate layer separated from the conductive signal pads by a dielectric material.

5. The method of claim 4 wherein capacitively coupling a test plate further comprises decoupling the test plate from a voltage reference and coupling the test plate to a receiving circuit generating a test signal in response to detecting the data signals at the test plate.

6. The method of claim 1 wherein evaluating the data signal detected by the test plate comprises:

generating a test signal in response to detecting the data signal at the test plate;

coupling the test signal to a test terminal of the integrated circuit; and

coupling test equipment to the test terminal to receive the test signal.

7. The method of claim 1 wherein the integrated circuit comprises a memory device.

8. The method of claim 1 wherein evaluating detected data signal comprises comparing the detected data signal to an expected data signal.

9. A method of testing an integrated circuit having a plurality of signal terminals, the method comprising:

applying a data signal to one of the plurality of signal terminals;

detecting the data signal at a test plate formed in proximity of the signal terminals to be capacitively coupled with the plurality of signal terminals; and

evaluating the detected data signal against a test criteria.

10. The method of claim 9 wherein applying a data signal, detecting the data signal, and evaluating the detected data signal are repeated for each signal terminal of the plurality.

11. The method of claim 9 applying the data signal to one of the plurality of signal terminals comprises generating a data signal representing pseudo-random data and driving the data signal on the signal terminal.

12. The method of claim 9 wherein evaluating the detected data signal comprises determining functionality of a transmitter applying the data signal to the signal terminal and integrity of a capacitor through which the signal terminal is capacitively coupled.

13. The method of claim 9 wherein evaluating the detected data signal comprises comparing the detected data signal to an expected data signal.

14. The method of claim 9 wherein the integrated circuit is formed on a semiconductor die, the test plate is formed from a conductive plate layer formed on the semiconductor die, and the signal terminals are formed from conductive signal pads positioned in proximity to the conductive plate layer, the conductive plate layer separated from the conductive signal pads by a dielectric material, and detecting the data signal at the test plate comprises decoupling the test plate from a voltage reference and coupling the test plate to a receiving circuit generating a test signal in response to detecting the data signals at the test plate.

15. The method of claim 9 wherein evaluating the data signal detected by the test plate comprises:

generating a test signal in response to detecting the data signal at the test plate;

coupling the test signal to a test terminal of the integrated circuit; and

coupling test equipment to the test terminal to receive the test signal.

16. The method of claim 9, further comprising placing the remaining signal terminals in a high-impedance state.

17. A method of testing an integrated circuit having a plurality of signal terminals from which data is provided over a corresponding plurality of capacitively coupled signal lines, the method comprising:

capacitively coupling a test plate to the plurality of signal terminals;

commanding the integrated circuit to generate a data signal at one of the plurality of signal terminals;

evaluating the data signal detected at the test plate in response to the generation of the data signal by the integrated circuit; and

repeating the commanding and evaluating for each of the plurality of signal terminals.

18. The method of claim 17 wherein the integrated circuit is formed on a semiconductor die and capacitively coupling a test plate comprises:

forming the test plate from a conductive plate layer formed on the semiconductor die; and

forming the plurality of signal terminals from conductive signal pads in proximity to the conductive plate layer, the conductive plate layer separated from the conductive signal pads by a dielectric material.

19. The method of claim 18 wherein capacitively coupling a test plate further comprises decoupling the test plate from a voltage reference and coupling the test plate to a receiving circuit generating a test signal in response to detecting the data signals at the test plate.

20. The method of claim 17 wherein evaluating the data signal detected by the test plate comprises:

generating a test signal in response to detecting the data signal at the test plate;

coupling the test signal to a test terminal of the integrated circuit; and

coupling test equipment to the test terminal to receive the test signal.

21. The method of claim 17 wherein evaluating the data signal comprises determining functionality of a transmitter applying the data signal to the signal terminal and integrity of a capacitor through which the signal terminal is capacitively coupled.

22. The method of claim 17 wherein evaluating the data signal comprises comparing the detected data signal against an expected data signal.

23. The method of claim 17 wherein commanding the integrated circuit to generate a data signal comprises commanding the integrated circuit to generate a data signal representing pseudo-random data.

24. The method of claim 17, further comprising placing the remaining data terminals of the plurality in a high impedance state.

25. A method of evaluating an integrated circuit having a plurality of data terminals at which data signals are received, the method comprising:

capacitively coupling a test plate to a plurality of signal terminals at which data signals are received;

transmitting a data signal from the test plate to one of the plurality of signal terminals; and

evaluating the data signal detected by at the signal terminal against a test criteria.

26. The method of claim 25, further comprising placing the remaining data terminals of the plurality in a high-impedance state.

27. The method of claim 25 wherein the receiving signal terminal is a first signal terminal, and the method further comprises:

ceasing reception of the data signal from the first signal terminal;

transmitting a data signal from the test plate to another one of the plurality of signal terminals; and

evaluating the data signal detected by other signal terminal against the test criteria.

28. The method of claim 25 wherein the integrated circuit is formed on a semiconductor die and capacitively coupling a test plate comprises:

forming the test plate from a conductive plate layer formed on the semiconductor die; and

forming data terminals from conductive signal pads and in proximity to the conductive plate layer, the conductive plate layer separated from the conductive signal pads by a dielectric material.

29. The method of claim 28 wherein capacitively coupling a test plate further comprises decoupling the test plate from a voltage reference and coupling the test plate to a transmitting circuit generating a test signal in response to detecting an input test signal.

30. The method of claim 25 wherein evaluating the data signal detected by the data terminal comprises:

generating a test signal applied to the test plate;

coupling the test signal detected at the data terminal to a test terminal of the integrated circuit; and

coupling test equipment to the test terminal to receive the test signal.

31. The method of claim 25 wherein the integrated circuit comprises a memory device.

32. The method of claim 25 wherein evaluating detected data signal comprises comparing the detected data signal to an expected data signal.

33. A test apparatus for an integrated circuit having a plurality of capacitively coupled signal terminals to which a corresponding plurality of transmitters are coupled, the transmitters applying a data signal to a respective signal terminal, the test apparatus comprising:

a test plate to capacitively couple to the signal terminals of the integrated circuit;

a test receiver circuit coupled to the test plate to receive and output the data signal detected at the test plate capacitively coupled to the signal terminals; and

a test unit coupled to the test receiver circuit to evaluate the detected data signal against test criteria.

34. The test apparatus of claim 33 wherein the test receiver comprises a buffer circuit.

35. The test apparatus of claim 33 wherein the test unit comprises test circuitry to determine the functionality of the transmitter applying the data signal to the signal terminal and the integrity of a capacitor through which the signal terminal is capacitively coupled.

36. The test apparatus of claim 33 wherein the test unit comprises test circuitry to compare the detected data signal against an expected data signal.

37. A test apparatus for testing a semiconductor device having a plurality of signal terminals from which a corresponding plurality of data signals are transmitted, the test apparatus comprising:

a test plate for capacitively coupled to the signal terminals to detect transmitted data signals; and

a test engine coupled to the capacitively coupled test plate to evaluate data signals detected by the test plate from a signal terminal transmitting the data signal, the test engine commanding the semiconductor device to transmit in sequence a respective data signal from each

of the plurality of signal terminals and further evaluating the respective detected data signals against test criteria.

38. The test apparatus of claim 37 wherein the semiconductor device is formed on a semiconductor die and the test plate comprises a conductive plate layer formed on the semiconductor die and the plurality of signal terminals comprises conductive signal pads formed in proximity to the conductive plate layer, the conductive plate layer separated from the conductive signal pads by a dielectric material.

39. The test apparatus of claim 38 wherein the semiconductor device further comprises a test circuit for decoupling the test plate from a voltage reference and coupling the test plate to a receiving circuit generating a test signal in response to detecting the data signals at the test plate.

40. The test apparatus of claim 39 wherein the test signal is coupled to a test terminal of the semiconductor device and the test engine is coupled to the test terminal to receive the test signal.

41. The test apparatus of claim 37, further comprising a test receiver electrically coupled between the test plate and the test engine, and the test receiver comprises a buffer circuit.

42. The test apparatus of claim 37 wherein the test engine comprises test circuitry to determine the functionality of transmitters applying a data signal to a respective signal terminal and the integrity of capacitors through which the signal terminals are capacitively coupled to the test plate.

43. The test apparatus of claim 37 wherein the test engine comprises test circuitry to compare the detected data signals against expected data signals.

44. A test apparatus for an integrated circuit having a plurality of capacitively coupled signal terminals to which a corresponding plurality of receivers are coupled, the receivers generating a respective data signal in response to detecting a respective input data signal, the test apparatus comprising:

a test plate to capacitively couple to the signal terminals of the integrated circuit;

a test transmitter circuit coupled to the test plate to transmit a data signal to at least one of the signal terminals through the test plate; and

a test unit coupled to the test signal terminals to evaluate the detected data signal against test criteria.

45. The test apparatus of claim 44 wherein the test transmitter comprises a buffer circuit.

46. The test apparatus of claim 44 wherein the test unit comprises test circuitry to determine the functionality of the receivers coupled to the signal terminals and the integrity of a capacitor through which the signal terminal is capacitively coupled.

47. The test apparatus of claim 44 wherein the test unit comprises test circuitry to compare the detected data signal against an expected data signal.